What is claimed is:

1. A method of forming multi-layers for manufacturing a thin film transistor (TFT), comprising:

forming a first layer on a transparent substrate using a first physical vapor deposition; and

sequentially forming a second layer using a second physical vapor deposition on the first layer without breaking vacuum.

2. The method of claim 1, wherein the physical vapor deposition for forming the first layer comprises pulsed-DC or RF sputtering.

3. The method of claim 1, wherein the first layer is silicon dioxide.

4. The method of claim 3, wherein the second layer is amorphous silicon.

5. The method of claim 1, wherein said forming a first layer is performed by sputtering using a first target comprising a silicon material selected from the group consisting of polysilicon and single-crystal silicon having a predetermined resistivity.

6. The method of claim 5, wherein the first layer is silicon dioxide and is sputter deposited from the first target with an oxygen reactive gas.

7. The method of claim 5, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen and He.

8. The method of claim 5, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen and H_2.

9. The method of claim 5, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen, He, and H_2.

10. The method of claim 5, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen and any one of Ar, Ne, or Kr.

11. The method of claim 5, wherein the first layer is silicon dioxide and is sputter deposited from the first target with a reactive gas mixture comprising oxygen, He, and any one of Ar, Ne, or Kr.

12. The method of claim 11, wherein the reactive gas mixture comprises oxygen, He and Ar, and wherein a ratio of Ar in He is between approximately 3-20% atomic?

13. The method of claim 5, wherein the predetermined resisvity R1 is in a range of approximately 1-50 Ohm-cm.

14. The method of claim 1, wherein said forming a first layer is performed by sputtering using a first target comprising silicon dioxide.

15. The method of claim 1, wherein said forming a second layer is performed by sputtering using a target formed of a material selected from the group consisting of single crystalline silicon and polycrystalline silicon.

16. The method of claim 1, wherein the physical vapor deposition for forming the second layer comprises regular-DC, pulsed DC or RF sputtering.

17. A thin film transistor, comprising:

a transparent substrate;

a first layer formed on the substrate using a first physical vapor deposition; and

a second layer formed sequentially on the first layer using a second physical vapor deposition, without breaking vacuum.

18. The thin film transistor of claim 17, wherein the first layer is formed using pulsed-DC or RF sputtering.

19. The thin film transistor of claim 17, wherein the first layer is silicon dioxide.

20. The thin film transistor of claim 19, wherein the second layer is amorphous silicon.

21. A poly-Si thin film transistor, comprising:

a transparent substrate;

a first layer formed on the substrate using a physical vapor deposition; and

a second layer formed sequentially on the first layer, using the physical vapor deposition and an annealing process for crystallization, without breaking vacuum.

22. The thin film transistor of claim 21, wherein the physical vapor deposition for forming the first layer comprises pulsed-DC or RF sputtering.

23. The thin film transistor of claim 21, wherein the first layer is silicon dioxide.

24. The thin film transistor of claim 23, wherein the second layer is polycrystalline silicon.

25. A display device, comprising:

a transparent substrate;

a first layer formed on the substrate using a first physical vapor deposition; and

a second layer formed sequentially on the first layer using a second physical vapor deposition, without breaking vacuum.

26. The device of claim 25, wherein the first layer is formed using pulsed-DC or RF sputtering.

27. The device of claim 25, wherein the first layer is silicon dioxide.

28. The device of claim 27, wherein the second layer is amorphous silicon.